

**What Is Claimed Is:**

1        1. A data recovery circuit for recovering an m-bit data  
2        stream from an n-bit data stream, said data recovery circuit,  
3        comprising:  
4        an n-bit data reconstruction circuit receiving said  
5        n-bit data stream, said n-bit data reconstruction  
6        circuit selecting a data boundary from a plurality  
7        of boundary selection candidates in response to a  
8        boundary selection signal and producing a  
9        reconstructed n-bit data stream based on said data  
10       boundary;  
11       a first-in first-out (FIFO) buffer circuit coupled to  
12       an output of said n-bit data reconstruction circuit,  
13       said first-in first-out buffer circuit including a  
14       register and a write and read control circuit for  
15       controlling an n-bit write operation and an m-bit  
16       read operation of said register to receiving said  
17       reconstructed n-bit data stream and producing said  
18       m-bit data stream; and  
19       a detection circuit coupled to an output of said FIFO  
20       buffer circuit, said detection circuit detecting said m-bit  
21       data stream and accordingly producing said boundary  
22       selection signal.

1       2. The data recovery circuit of claim 1, wherein n is  
2       a positive integer power of 2.

1       3. The data recovery circuit of claim 1, wherein n is  
2       smaller than m.

1       4. The data recovery circuit of claim 1, wherein m is  
2       not a multiple of n.



1        5. The data recovery circuit of claim 1, wherein said  
2        register having a number of bits equal to the least common  
3        multiple of n and m.

1        6. The data recovery circuit of claim 1, wherein a ratio  
2        of a transmission rate of said m-bit data stream to that  
3        of said n-bit data stream is n : m.

1        7. The data recovery circuit of claim 1, wherein said  
2        n-bit data reconstruction circuit comprises:  
3        an input register for temporarily storing data from said  
4        n-bit data stream;  
5        a data reconstruction multiplexer coupled to said input  
6        register, said data reconstruction multiplexer  
7        selecting said data boundary from said plurality of  
8        boundary selection candidates in response to said  
9        boundary selection signal and selecting  
10       reconstructed data from the data stored in said input  
11       register based on said data boundary; and  
12       an output register coupled to said data reconstruction  
13       multiplexer, said output register temporarily  
14       storing the reconstructed data selected by said data  
15       reconstruction multiplexer and producing said  
16       reconstructed n-bit data stream.

1        8. The data recovery circuit of claim 1, wherein said  
2        detection circuit is incorporated in a decoder, which is  
3        operable to decode said m-bit data stream for output.

1        9. The data recovery circuit of claim 1, wherein said  
2        write and read control circuit comprises:  
3        a write controller for controlling the n-bit write  
4        operation of said register and producing a write



5           pointer indicator signal; and  
6       a read controller for controlling the m-bit read  
7       operation of said register based on said write  
8       pointer indicator signal.

1       10. A data receiving system, comprising:  
2       a plurality of data recovery circuits, each for  
3       recovering one of a plurality of m-bit data streams  
4       from one of a plurality of n-bit data streams and  
5       decoding said one of a plurality of m-bit data streams  
6       into one of a plurality of decoded data streams, each  
7       of said data recovery circuit comprising:  
8       an n-bit data reconstruction circuit receiving said  
9       n-bit data stream, said n-bit data  
10      reconstruction circuit selecting a data boundary  
11      from a plurality of boundary selection  
12      candidates in response to a boundary selection  
13      signal and producing a reconstructed n-bit data  
14      stream based on said data boundary;  
15      a first-in first-out (FIFO) buffer circuit coupled  
16      to an output of said n-bit data reconstruction  
17      circuit, said first-in first-out buffer circuit  
18      including a register and a write and read control  
19      circuit for controlling an n-bit write operation  
20      and an m-bit read operation of said register to  
21      receiving said reconstructed n-bit data stream  
22      and producing said m-bit data stream; and  
23      a decoder coupled to an output of said FIFO buffer  
24      circuit, said decoder including a detection  
25      circuit for detecting said m-bit data stream and  
26      accordingly producing said boundary selection  
27      signal, said decoder decoding said m-bit data



28 stream into said decoded data stream upon said  
29 detection circuit detects a correct condition of  
30 said m-bit data stream; and  
31 a cycle alignment circuit receiving said plurality of  
32 decoded data streams from said plurality of data recovery  
33 circuits, said cycle alignment circuit aligning phases of  
34 said plurality of decoded data streams to synchronize said  
35 plurality of decoded data streams.

1 11. The data receiving system of claim 10, wherein said  
2 cycle alignment circuit comprises a plurality of delay  
3 lines, each for receiving one of said plurality of decoded  
4 data streams, each of said plurality of delay lines  
5 including a plurality of delay elements and a selector  
6 coupled to outputs of said plurality of delay elements to  
7 select one of said outputs of said plurality of delay  
8 elements as an aligned output.

1 12. A data recovery method for recovering an m-bit data  
2 stream from an n-bit data stream, said data recovery method  
3 comprising the steps of:  
4 receiving said n-bit data stream;  
5 selecting a data boundary from a plurality of boundary  
6 selection candidates in response to a boundary  
7 selection signal and producing a reconstructed n-bit  
8 data stream based on said data boundary;  
9 performing an n-bit write operation to store said  
10 reconstructed n-bit data stream into a register and  
11 performing an m-bit read operation to retrieve said  
12 m-bit data stream from said register, a ratio of a  
13 rate of said write operation to that of said read  
14 operation being  $m : n$ ; and  
15 detecting whether or not said m-bit data stream conforms



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to a predetermined format and accordingly producing

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said boundary selection signal.